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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,061	BANERJEE ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35,37,38 and 40-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35,37,38 and 40-46* is/are rejected.

7)☒ Claim(s) *35 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35, 37-38, and 40-46 have been considered. Claims 36 and 39 are cancelled as per Applicants' request. Claims 23-30, 35, 37-38, and 44-46 are amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 19 March 2009.

Claim Objections

3. Claims 35 and 38 are objected to because of the following informalities:

a. Referring to claim 35, please correct lines 13-14 from "set architecture for each of the first instruction and the second instruction. instruction," to read --set architecture for each of the first instruction and the second instruction~~.~~ ~~**instruction**~~,--. Appropriate correction is required.

b. Referring to claim 38, please correct line 6 from "belonging to a second instruction set. set, and" to read -- belonging to a second instruction set~~. **set**~~, and --. Appropriate correction is required.

Response to Arguments

4. Examiner withdraws the objections to claims 23-30 and 45-46 in view of the arguments.

5. Applicant's arguments filed 19 March 2009 have been fully considered but they are not persuasive.

6. Applicants' argue in essence on pages 16-17 "While parallel operation may be one goal, the Examiner's conclusion ignores other important goals in processor design including

simplifying circuit design, minimizing power consumption and minimizing component footprint, each of which would likely be complicated by the proposed combination. Moreover, technical difficulties will surely arise with duplication of components required by the proposed combination…Applicants respectfully submit that without addressing at least these issues the Examiner has failed to establish a *prima facie* case of obviousness…" This has not been found persuasive. Goals are established and prioritized by designers. Different goals are more important to different designers. Simply having different goals and motivations does not invalidate the a rejection. These general arguments are mere assertions and literally implanting one invention to another. There is no evidence to support applicants' assertions regarding the technical difficulties. Without evidence, these assertions are assumed to be mere allegations. In response to applicant's argument that literally incorporating Miller into Trivedi, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

7. Applicants' argue in essence on page 17-21 "…Thus, claim 1 requires at least two recoders, each of which maps an instruction from one encoded state to another encoded state…" This has not been found persuasive. A recoder, according to the claim language, simply converts an instruction from one state to another state. As such, a recoder can be anything that changes the representative state of an instruction. In Trivedi, the translator 302c, decoder 302b, and detector 306 all take the instruction and convert that instruction information into different forms,

such as the speculative wake-up signal from the detector, another instruction format from the translator, and execution signals from the decoder. Consequently, there are multiple recoders linked together.

8. Applicants' argue in essence on pages 18-21 "As recited in claim 1, the first recoder 'passed information regarding a first instruction…to the second recoder.' As further recited…the second recoder uses 'the passed information to form a recoded instruction belonging to a second instruction set architecture.'" This has not been persuasive. When the detector 306 detects that an instruction set mode change from an instruction, this information is passed to the translator, which then knows to translate instructions of a second instruction set architecture being fetched. Hence, the detector 306, i.e. first recoder, passes information regarding a first instruction set to the translator 302c, i.e. second recoder, so the translator knows to for a recoded instruction.

9. Applicants' argue in essence on pages 19-21 "…Applicants respectfully assert that such translation does not teach or suggest features of claim 31 set forth above…" This has not been found persuasive. Since no specific arguments have been provided as to why it is believed the highlighted limitations of claim 31 are not taught, the Examiner can merely assert that the limitations are taught as set forth in the rejection below. For example, Trivedi has taught fetching expandable instruction in cited sections, such as Figure 3, element 302a and column 4, lines 34-42. Dispatching the instructions as shown in Figure 3 via MUX 301 and decoder 302b and associated specification text. Generating at least one information bit based on the expand instruction by detector 306 and associated specification text. Recoding the instruction by translator 302c and associated specification text.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-4, 7-12, 15-20, 23-26, 29-41, 43, and 45-46 rejected under 35 U.S.C. 103(a) as being unpatentable over Trivedi (U.S. Patent No. 6,430,674) in view of Miller (U.S. Patent No. 6,405,303).

12. As per claim 1, Trivedi discloses an instruction fetch unit for a processor (fig. 3 reference 302a, comprising: a first recoder (fig. 3 reference 306 or "circuitry" discussed on col 4 lines 17-33); and a second recoder coupled to the first recoder (fig. 3 reference 302c), wherein the first recoder passes information regarding (fig. 3 "speculative wake up" or "mode select signal" from col 4 lines 17-33) a first instruction belonging to a first instruction set architecture to the second recoder, and the second recoder recodes a second instruction belonging to the first instruction set architecture using the passed information to form a recoded instruction belonging to a second instruction set architecture (col 4 lines 17-33).

13. Trivedi fails to disclose that the first recoder maps an instruction from one encoded state to another encoded state.

14. Miller discloses expanding the pipeline by duplicating, for example, decode and execution units in order to operate in a more parallel fashion (Fig. 4 20A-20N; Fig. 5 20A-20N; Col 3. lines 9-16).

15. Trivedi would have been motivated to incorporate this functionality to improve parallelization. Indeed, Trivedi has contemplated similar improvements (Col. 4 lines 6-10).

16. It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Trivedi and incorporate the improved parallelization of Miller by duplicating at least the decode units. Relating this invention to Trivedi, in Fig. 3 the Translator 302c is matched to the Decoder 302b. Therefore, a duplication of the Decoder would logically incorporate a duplication of the Translator, allowing (at least) two of each. Moreover, as a matter of interpretation, one of the two translators is interpreted to include the Detector 306. Indeed, the Detector would be interpreted as being part of Translator 1, which would pass wake-

up information to both Translators, including Translator 2. All elements of the claim are then satisfied.

17. As per claim 2, Trivedi/Miller discloses the instruction fetch unit of claim 1, further comprising: an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder (col 3 line 62 to col 4 lines 10).

18. As per claim 3, Trivedi/Miller discloses the instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits. (col 3 lines 33-46).

19. As per claim 4, Trivedi/Miller discloses the instruction fetch unit of claim 3, wherein each instruction of the first instruction set has 16-bits and each instruction of the second instruction set has 32-bits. (col 3 lines 33-46).

20. As per claim 7, Trivedi/Miller discloses the instruction fetch unit of claim 3, wherein the first instruction set includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction. (Col. 4 lines 17-33).

21. As per claim 8, Trivedi/Miller discloses the instruction fetch unit of claim 7, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction. (Col. 4 lines 17-33).

22. As per claim 9, Trivedi/Miller has taught a processor employing the fetch unit of claim 1, consequently claim 9 is rejected for the same reasons set forth in the rejection of claim 1 above.

23. As per claim 10, Trivedi/Miller has taught a processor employing the fetch unit of claim 2, consequently claim 10 is rejected for the same reasons set forth in the rejection of claim 2 above.

24. As per claim 11, Trivedi/Miller has taught a processor employing the fetch unit of claim 3, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 3 above.

25. As per claim 12, Trivedi/Miller has taught a processor employing the fetch unit of claim 4, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 4 above.

26. As per claim 15, Trivedi/Miller has taught a processor employing the fetch unit of claim 7, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 7 above.

27. As per claim 16, Trivedi/Miller has taught a processor employing the fetch unit of claim 8, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 8 above.

28. As per claim 17, Trivedi/Miller has taught a processing system employing the fetch unit of claim 1, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 1 above.

29. As per claim 18, Trivedi/Miller has taught a processing system employing the fetch unit of claim 2, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 2 above.

30. As per claim 19, Trivedi/Miller has taught a processing system employing the fetch unit of claim 3, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 3 above.

31. As per claim 20, Trivedi/Miller has taught a processing system employing the fetch unit of claim 4, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

32. As per claim 23, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 1, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 1 above.

33. As per claim 24, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 2, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 2 above.

34. As per claim 25, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 3, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 3 above.

35. As per claim 26, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 4, consequently claim 26 is rejected for the same reasons set forth in the rejection of claim 4 above.

36. As per claim 29, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 7, consequently claim 29 is rejected for the same reasons set forth in the rejection of claim 7 above.

37. As per claim 30, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 8, consequently claim 30 is rejected for the same reasons set forth in the rejection of claim 8 above.

38. As per claim 31, Trivedi/Miller discloses a method for recoding instructions for execution by a computer readable medium comprising a microprocessor core, comprising:

a. fetching an expand instruction (col 4 lines 34-42) and an expandable instruction (col 4 lines 34-42) from an instruction cache (col 3 line 62 to col 4 lines 10);

b. dispatching the expand instruction to a first recoder and dispatching the expandable instruction to a second recoder; (col 4 lines 17-33)

c. generating at the first recoder at least one information bit based on the expand instruction; (col 4 lines 17-33); and

d. recoding the expandable instruction using the at least one information bit generated to form a recoded instruction belonging to a second instruction set architecture. (Col. 4 lines 17-33)

39. As per claim 32, Trivedi/Miller discloses the method of claim 31, wherein step (a) comprises:

i. fetching the expand instruction during a first clock cycle of the computer readable medium comprising a microprocessor core; and

ii. fetching the expandable instruction during a subsequent clock cycle of the computer readable medium comprising a microprocessor core (fig. 3 and col 4 lines 17-33).

40. As per claim 33, Trivedi/Miller discloses the method of claim 31, wherein the at least one information bit based on the expand instruction is generated at the first recoder during a first clock cycle of the processor, and the expandable instruction is recoded at the second recoder during a second clock cycle of the computer readable medium comprising a microprocessor core (col 4 lines 17-33 and fig. 3).

41. As per claim 34, Trivedi/Miller discloses the method of claim 33, further comprising a step between steps (c) and (d) of:

a. storing the at least one information bit generated at the first recoder in an information storage buffer. (col 4l lines 17-33).

42. As per claim 35, Trivedi/Miller discloses a method for recoding instructions for execution by a processor, comprising:

a. fetching a plurality of instructions from an instruction cache (col 3 line 62 to col 4 lines 10), wherein the plurality of instructions includes a first instruction belonging to a first instruction set architecture and a second instruction being long to the first instruction set architecture, and the first instruction is different from the second instruction (col 4 lines 17-33)

b. dispatching the first instruction to a first recoder and the second instruction to a second recoder; (fig. 3)

c. and recoding the first and second instructions within a single clock cycle so as to form recoded instructions belonging to a second instruction set architecture for each of the first instruction and the second instruction (col 4 lines 17-33),

d. wherein the recoding of the second instruction is performed using information from the first recoder (col. 4 lines 17-33).

43. As per claim 36, Trivedi/Miller discloses the method of claim 35, wherein the recoding of the second instruction is performed using information from the first instruction. (Col. 4 lines 17-33).

44. As per claim 37, Trivedi/Miller discloses the method of claim 35, further comprising: forwarding information from the first recoder to the second recoder, such information used by the second recoder to perform a recoding operation. (Col. 4 lines 17-33).

45. As per claim 38, Trivedi/Miller discloses an instruction fetch unit for a processor, comprising:

a. a plurality of recoders that operate in parallel, each recoder mapping an instruction from one encoding state to another encoding state (Fig. 3 wake up signal, fig. 3 reference 302c and col 4 lines 17-33);

b. wherein the recoders recode instructions belonging to a first instruction set architecture within a single clock cycle so as to form recoded instructions belonging to a second instruction set (col 4 lines 17-33), and

c. wherein one of the recoders recodes one instruction using information from another recoder (col. 4 lines 17-33).

46. As per claim 39, Trivedi/Miller discloses the instruction fetch unit of claim 38, wherein the second recoder recodes the second instruction using information from the first instruction. (Col. 12 lines 21-31).

47. As per claim 40, Trivedi/Miller discloses the instruction fetch unit of claim 39, wherein the first recoder is coupled to the second recoder. (fig. 3).

48. As per claim 41, Trivedi/Miller discloses the instruction fetch unit of claim 1, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction. (col 3 lines 33-46).

49. As per claim 43, Trivedi/Miller has taught a processor employing the fetch unit of claim 41, consequently claim 43 is rejected for the same reasons set forth in the rejection of claim 41 above.

50. As per claim 45, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 41, consequently claim 45 is rejected for the same reasons set forth in the rejection of claim 41 above.

51. As per claim 46, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 42, consequently claim 46 is rejected for the same reasons set forth in the rejection of claim 42 above.

52. Claims 5, 6, 13, 14, 21, 22, 27, 28, 42, and 44 rejected under 35 U.S.C. 103(a) as being unpatentable over Trivedi/Miller over Common Art.

53. As per claim 5, Trivedi/Miller discloses the instruction fetch unit of claim 3, wherein the first instruction set includes an expand instruction used to enlarge a field of an expandable instruction of the first instruction set, (col 4 lines 17-33) and wherein the first recoder passes at

least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction. (col 4 lines 17-33 and col 3 lines 33-46).

54. Trivedi fails to disclose that the expandable portion is the immediate field.

55. Examiner takes Official Notice that expanding an instruction architecture (for example, from 32 to 64 bits) often includes expanding the immediate field.

56. Trivedi would have been motivate to utilize this technique to expand the architecture in such a way that the immediate field contains larger numbers, which increases the flexibly of coding.

57. It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Trivedi and incorporate the immediate field expansion of common art.

58. As per claim 6, Trivedi/Miller discloses the instruction fetch unit of claim 5, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction. (col 4 lines 17-33 and col 3 lines 33-46).

59. As per claim 13, Trivedi/Miller has taught a processor employing the fetch unit of claim 5, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 5 above.

60. As per claim 14, Trivedi/Miller has taught a processor employing the fetch unit of claim 6, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 6 above.

61. As per claim 21, Trivedi/Miller has taught a processing system employing the fetch unit of claim 5, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 5 above.

62. As per claim 22, Trivedi/Miller has taught a processing system employing the fetch unit of claim 6, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 6 above.

63. As per claim 27, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 5, consequently claim 27 is rejected for the same reasons set forth in the rejection of claim 5 above.

64. As per claim 28, Trivedi/Miller has taught a computer readable medium comprising a microprocessor core employing the fetch unit of claim 6, consequently claim 28 is rejected for the same reasons set forth in the rejection of claim 6 above.

65. As per claim 42, Trivedi/Miller discloses the instruction fetch unit of claim 41, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field. (col 3 lines 33-46).

66. As per claim 44, Trivedi/Miller has taught a processor employing the fetch unit of claim 42, consequently claim 44 is rejected for the same reasons set forth in the rejection of claim 42 above.

Conclusion

67. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Ku, U.S. Patent Application Publication 2004/0024992, has taught translating and decoding multiple instruction sets.

b. Shelor, U.S. Patent Application Publications 2004/0199747 and 2004/0205322 and U.S. Patent Number 7,194,601, has taught multiple decoders.

c. Hammond et al., U.S. Patent Number 5,638,525, has taught multiple instruction set decoders.

d. Blomgren et al., U.S. Patent number 5,781,750, has taught multiple instruction set modes and translators and decoders for each modes.

e. O'Connor et al., U.S. Patent Number 6,961,843, has taught translating and decoding multiple instruction sets.

68. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

69. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

70. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

71. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

72. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183

5 July 2009